REMARKS

Claims 1-12, 14, 16 and 18-19 were presented for examination. Claims 1-12, 14, 16 and 18-19 were rejected. Applicant is hereby amending claims 1 and 12. Reconsideration of this application as amended, and allowance of all pending claims are hereby respectfully requested.

The Applicant would like to thank the Examiner for the interview conducted on September 20, 2004. In the interview, the Examiner clarified that the finality of the Office Action mailed May 12, 2004 had been withdrawn in view of the present Office Action and the accompanying new grounds of rejection.

Claim Objections

In the Office Action, claims 1 and 12 were objected to for informalities. Claims 1 and 12 are amended herein to address the Examiner's concerns. Reconsideration and withdrawal of the claim objections are respectfully requested.

Rejection under 35 U.S.C. § 103

Claims 1, 5, 12, 14, 16 and 18-19 were rejected under 35 U.S.C. § 103 as being unpatentable over Emma (U.S. Patent No. 5,619,665) in view of IBM (IBM Technical Disclosure Bulletin, "Instruction Cache Bypass During Cache Reload Operation," vol. 32). Applicant respectfully requests reconsideration and allowance of the claims in view of the following arguments. For at least the reasons stated below, a combination of Emma and IBM, even if proper, does not disclose or suggest the claimed invention.

The present invention, as recited in independent claim 1 for example, relates to an instruction translator for a processor. The translator receives a non-native architecture instruction

and translates the non-native architecture instruction into one or more corresponding translated instructions. An instruction cache is provided for temporarily storing the translated instruction(s). A selector provides an instruction to the processor for execution. The processor is configured to execute only native format instructions. The selector determines whether to provide a translated instruction from the instruction cache or a translated instruction from the translator.

Emma does not disclose or suggest an instruction translator that provides instructions to a processor that is "configured to execute instructions only in said first instruction architecture" as recited in independent claims 1 and 12 as amended. In contrast to the Applicant's claimed invention, Emma describes an arrangement for extending an instruction set architecture to encompass new instructions. In Emma, when a sequence of conventional instructions can be translated into extended architecture instructions, the resulting translated instructions are stored in the extended instruction (EI) cache (See Emma at FIG. 5 and col. 12, lines 17-23). In Emma, the processor may execute a conventional instruction or a translated instruction. One advantage of the claimed invention is that the processor receives instructions in the first instruction architecture (e.g., native format) and need not be capable of executing instructions in multiple instruction set architectures.

Even if the proposed combination of Emma and IBM were proper, the references do not disclose or suggest all the required claim elements. IBM discloses a cache bypassing technique, in which data from main memory is written into a cache and also is stored in an instruction buffer for allowing an instruction unit to execute the data immediately upon a cache miss. Neither Emma nor IBM disclose or suggest that the processor is configured to execute instructions only in said first instruction architecture as presently claimed.

Regarding independent claim 16, the proposed combination of Emma and IBM, even if proper, does not disclose or suggest all the required claim elements. Claim 16 requires a processor, a bus, a first and second instruction memories, a first instruction storage unit and an instruction translator. The second instruction memory includes a second instruction storage unit, and an instruction reading circuit. The first instruction memory stores instructions that have been translated into a first architecture and the second instruction memory also stores instructions in the first architecture. As described above, neither Emma nor IBM, individually or in combination, discloses or suggests providing the processor with instructions having a single instruction architecture.

In addition, the Office Action states that one of ordinary skill in the art would recognize that the instructions from the main memory including the translated instructions to be stored in the cache should be applied from the translator before the storage. However, IBM does not describe the direct application before the storage. As described above, in IBM, the instructions from the main memory are stored into the cache and also into the instruction buffer. Therefore, the proposed combination of references, even if proper, does not result in the claimed invention.

Dependent claims 5, 14 and 18-19 should also be considered allowable over the proposed combination. The dependent claims include additional patentable recitations that are not disclosed in the proposed combination of references. Reconsideration and withdrawal of the rejection of claims under 35 U.S.C. §103(a) are respectfully requested.

Dependent claims 2-4 and 6-11 were rejected under 35 U.S.C. § 103 as being unpatentable over Emma in view of IBM, Dickol et al. (U.S. Patent No. 5,875,336, Goettelmann et al. (U.S. Patent No. 5,313,614), Gregor (U.S. Patent No. 5,023,776), and Schacham et al. (UK Patent Application GB220481A) in various combinations. These claims depend from independent base claim 1 and should also be considered allowable over the proposed combination.

As described above, Emma does not disclose or suggest an instruction translator that provides instructions to a processor that is "configured to execute instructions only in said first instruction architecture" as recited in independent claim 1 as amended. Even if proper, the proposed combination does not disclose the claimed invention, as Emma is deficient for at least the reasons described above. Applicant respectfully requests reconsideration and allowance of these claims.

Conclusion

Accordingly, it is believed that all pending claims are now in condition for allowance. Applicant therefore respectfully requests an early and favorable reconsideration and allowance of this application. If there are any outstanding issues which might be resolved by an interview or an Examiner's amendment, the Examiner is invited to call Applicant's representative at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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